

REMARKS/ARGUMENTS

Claims 8 and 18 were objected to because of informalities and/or defects.

Claims 1, 4, and 9-11 stand rejected under 35 U.S.C. 102(b) as being anticipated by Staab; claims 2 and 3 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Staab in view of Kluth; claims 5-7 and 17-20 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Staab in view of Williams; claim 8 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Staab in view of Ker.

Claim 1 has been amended to include the limitation of a diode circuit comprising back to back diodes conductively coupled to the source region. In forming the rejection to this limitation the examiner combines the Staab reference with the Williams reference. The Williams reference describes a back to back diode configuration between the circuit power supply and the circuit input. The instant invention is limited to SOI circuits and in particular describes back to back diodes connected between the transistor source and the transistor gate. There is nothing disclosed in the Staab reference that states or suggests that back to back diodes will work in the configuration of the instant invention. In a similar manner, The Williams reference does not anticipate the configuration of the instant invention and clearly does not describe any of the special requirements of SOI circuits. There is therefore no motivation to combine the back to back diodes of the Williams circuit which are connected between the circuit power supply and the circuit input, with the Staab reference which describes a SOI circuit. Amended claim 1 is therefore allowable over the cited art. Claims 2, 3, and 7 depend on claim 1 and therefore contain all the limitations of claim 1. Claims 2, 3 and 7 are therefore also allowable over the cited art.

Claim 8 has been amended to include the limitation of at least three diodes connected in series. This configuration is neither taught nor anticipated by the Staab reference. In forming the rejection to this limitation the examiner combined the Staab reference with the Ker reference. The Ker reference does not disclose connecting

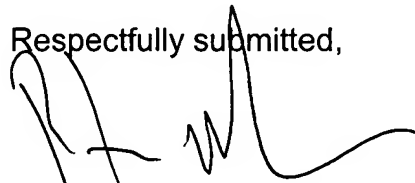
diodes between the gate and source. The Ker reference instead discloses connecting diodes between the circuit input and the various power supplies. There is nothing in the Ker reference that teaches or suggests that diodes can be connected between the gate and source of the SOI transistors. The Ker reference clearly teaches connecting the diodes between the circuit input and the various power supplies. As the examiner admits, there is nothing in the Staab reference that describes or suggests the use of multiple diodes. Therefore, the Staab reference and the Ker references cannot be properly combined under 35 U.S.C. 103 to properly reject amended claim 8. Amended claim 8 is therefore allowable over the cited art.

In light of the above, it is respectfully submitted that the present application is in condition for allowance, and notice to that effect is respectfully requested.

While it is believed that the instant response places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

To the extent necessary, Applicants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,

A handwritten signature in black ink, appearing to read 'Peter K. McLarty', with a long horizontal flourish extending to the right.

Peter K. McLarty
Attorney for Applicants
Reg. No. 44,923

Texas Instruments Incorporated
P.O. Box 655474, MS 3999
Dallas, TX 75265
(972) 917-4258